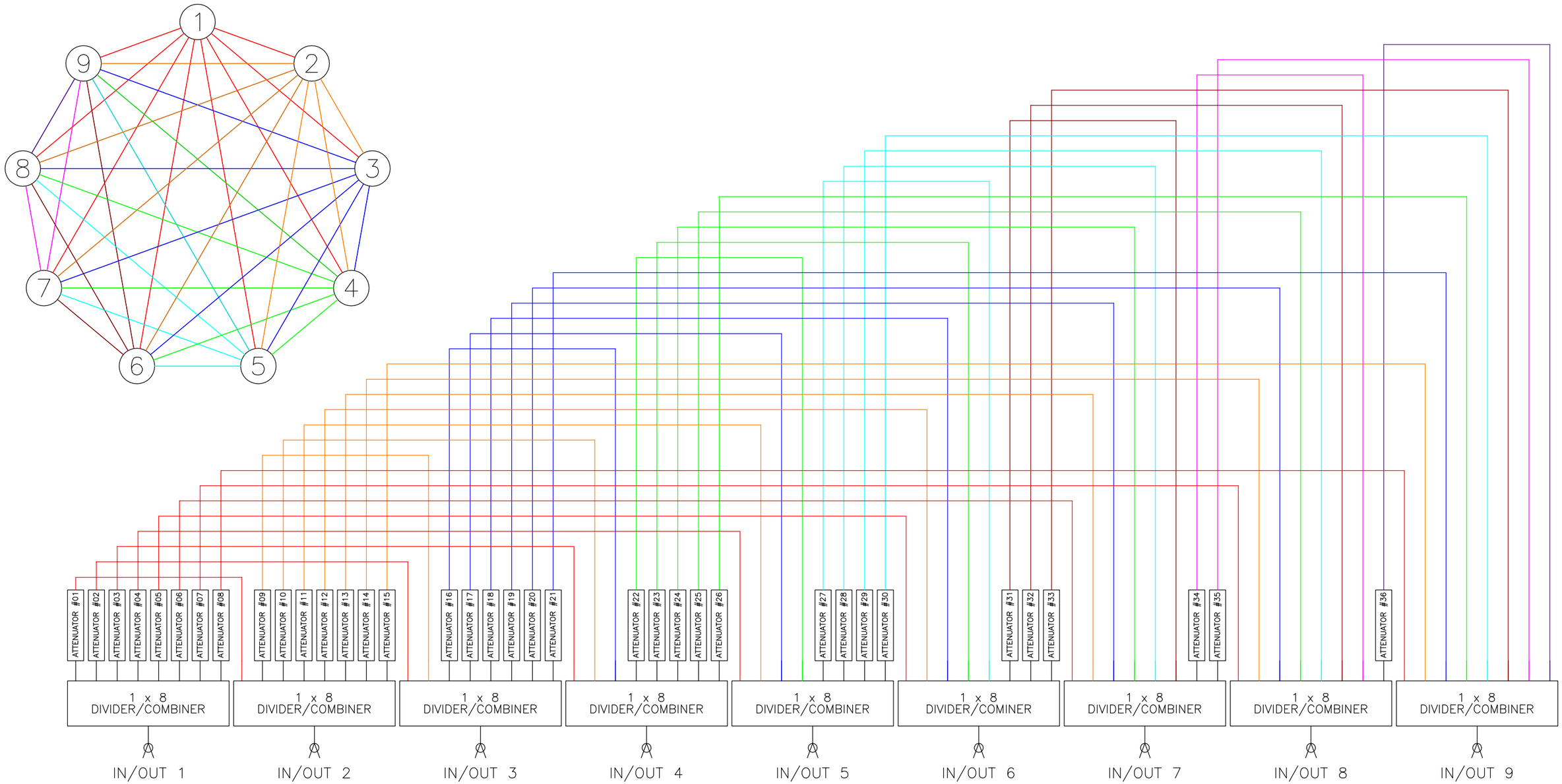

THIS IS A 9 PORT TRANSCEIVER TEST SYSTEM.
IT IS FULL FAN-OUT.
EVERY PORT CONNECTS TO EVERY OTHER PORT VIA 36 INTERNAL RF PATHS.
IT HAS AN ATTENUATOR ON EVERY RF PATH (36 TOTAL ATTENUATORS).

REV	ECN	DATE	BY	APPR
–	ISSUED	3-20-07	BZ	TEZ
A	14154	5-3-07	TRS	TEZ
B	14280	6-14-07	TRS	TEZ
C	16913	3-4-09	BZ	TEZ
D	21168	1-23-12	JZ	TRS
E	26712	6-13-16	DTS	TRS

JFW INDUSTRIES, INC.
www.jfwindustries.com PH: 317-887-1340

MATERIAL
PROPRIETARY INFORMATION
FINISH
ALL SURFACES ARE TO BE FREE OF BURRS, PITS, & SCRATCHES
MODEL 50PMA-XXX
SCALE
TOLERANCES .XX±.010 .XXX±.005 XX°±.5°
DESCRIPTION 9 PORT TRANSCEIVER TEST SYSTEM BLOCK DIAGRAM
DWG # 092-5356