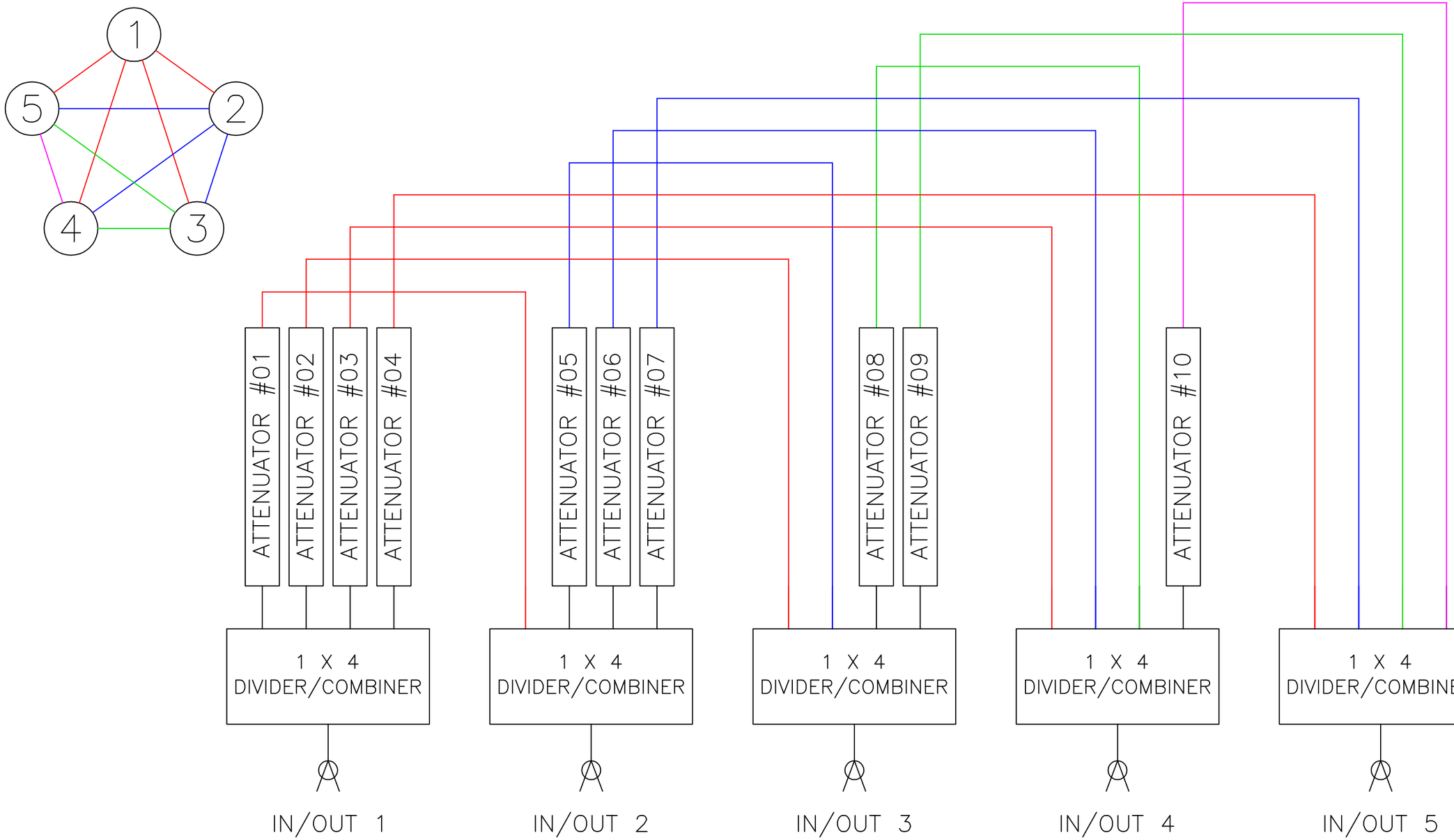

THIS IS A 5 PORT TRANSCEIVER TEST SYSTEM.
IT IS FULL FAN-OUT.
EVERY PORT CONNECTS TO EVERY OTHER PORT VIA 10 INTERNAL RF PATHS.
IT HAS AN ATTENUATOR ON EVERY RF PATH (10 TOTAL ATTENUATORS).

REV	ECN	DATE	BY	APPR
–	ISSUED	9-28-10	BZ	TEZ
A	21630	6-7-12	DTS	TRS
B	26712	6-13-16	DTS	TRS

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MATERIAL	PROPRIETARY INFORMATION
FINISH	ALL SURFACES ARE TO BE FREE OF BURRS, PITS, & SCRATCHES
MODEL / SCALE	TOLERANCES .XX±.010 .XXX±.005 XX°±.5°
DESCRIPTION: 5 PORT TRANSCEIVER TEST SYSTEM BLOCK DIAGRAM	DWG # 092-6730